Design, implementation and characterization of a PLL-based frequency synthesizer for the HF band

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Outline

1. Project Presentation
2. Phase Locked Loop
3. Frequency Synthesizer
4. State of the art
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Precedents and Justifications

- Communications = Need.
- Phase Locked Loop: applications in communications.
- Advantage of a PLL-based Frequency Synthesizer.
- Frequency band 26,957 MHz to 27,283 MHz.
Elaborate a PLL (Phase Locked Loop)-based Frequency Synthesizer for a specific band of HF. This Synthesizer will be able to be used in a Superheterodyne receiver.
Objectives

**General Objective**
Designing and implementing a PLL-based frequency synthesizer for the band of 26,502 MHz to 26,828 MHz with a frequency discrimination of 10 channels and a power output greater or equal to 0 dBm.

**Specifics Objectives**
- Simulate a PLL in the software “Microwave Office”.
- Characterize the PLL for the proposed application.
- Elaborate and test two prototypes of the application, being the second prototype a corrected version of the first.
- Appropriation of the design techniques for a PLL.
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Phase Locked Loops

Parts

Phase Detector
Low-Pass Filter
Voltage Controlled Oscillator (VCO).

Applications

Signal Processing.
First Application: in 1932, demodulation AM.
Linearized PLL model

- Phase Detector: Negative Feedback
- Voltage Controlled Oscillator: Integrator
- Filter: N-Order PLL

From http://tsc.unex.es/~ycampos
Phase Detector

\[ v_d(t) \approx K_d \left( \phi_r(t) - \phi_{out}(t) \right) \]

Implementations

- Analog Multiplier
- Commutating Multiplier
- Exclusive – OR Gate
- Sequential Detectors with Extended Range
Examples

CD4046

MC12181

From the National Semiconductor data sheet

From the Motorola data sheet
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Direct Synthesis

From http://tsc.unex.es/~ycampos
Indirect Synthesis

1. Synthesizer with static moduli

\[ f_{out} = \frac{M}{N} f_{ref} \]

From Thomas H. Lee. Planar Microwave Engineering.
Divider Logic: 2 counters, 1 prescaler

From Thomas H. Lee. Planar Microwave Engineering.
Synthesizer with dithering moduli

\[ N_{\text{eff}} = (N+1)(1/K) + N(1 - 1/K) = N + \frac{1}{K} \]

\[ f_{\text{out}} = N_{\text{eff}} f_{\text{ref}} = (N + \frac{1}{K}) f_{\text{ref}} \]

From Thomas H. Lee. Planar Microwave Engineering.
Combination Synthesizer

Offset Synthesizer

\[ f_{out} = f_{ref} + f_{offset} \]

From Thomas H. Lee. Planar Microwave Engineering.
Direct Digital Synthesis

Accumulator ACC, ROM Memory, DAC Converter

From Thomas H. Lee. Planar Microwave Engineering.
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VCOs better characteristics

Low levels phase noise

Integration with several technologies

PLLs and mixers Combination

Spurs reduction
Some Papers

• Seoncheol Kim and Youngsik Kim, A Fractional-N PLL Frequency Synthesizer Design, , Dept. of Information and Technology Eng., Handong Global University.

• Volodymyr Kratyuk, Pavan Kumar Hanumolu, Un-Ku Moon and Kartikeya Mayaram, A Low Spur Fractional-N Frequency Synthesizer Architecture, School of Electrical Engineering and Computer Science, Oregon State University.

• Michael Parle And Michael Peter Kennedy Comments on the effectiveness of the Szabo and Kolumban solution to false lock in Sampling PLL Frequency Synthesizer, Department of Microelectronic Engineering, University College Cork, Ireland.

Some Papers


• Alexander Chenakin, A Broadband, Low Phase Noise, Fast Switching PLL Frequency Synthesizer, Phase Matrix, Inc. San Jose, CA.

• Sau-Mou Wu and Wei-Liang Chen, A 5-ghz delta-sigma pll frequency synthesizer for WLAN applications, The Graduate School of Electrical Engineering, Yuan Ze University, Taiwan.

• Shaojun Wu, A Low-Noise Fast-Settling PLL Frequency Synthesizer for CDMA Receivers.

• Tie Sun, Chun Hui, A VCO with High Supply Noise Rejection and Its Application to PLL Frequency Synthesizer, Research institute of Micro/Nano science and technology, Shanghai Jiao Tong University, Shanghai, China.
Some Papers

• Haihong Ma, Xiaohong Tang, Fei Xiao, Chizhou Tan, Design and Analysis of the S-band PLL Frequency Synthesizer with Low Phase Noise, School of Electronic Engineering, University of Electronic Science and Technology of China, China.

• Haiyong Wang Guoliang Shou Nanjian Wu, An adaptive frequency synthesizer architecture reducing reference sidebands Beijing LHWT Microelectronics INC. Institute of Semiconductors, Chinese Academy of Sciences, China.


• Mücahit Kozak and Eby G. Friedman, Design and simulation of fractional-n pll frequency synthesizers, Department of Electrical and Computer Engineering, University of Rochester. New York.
Bibliography

